REMARKS

Reconsideration of the present application is respectfully requested. Claims 1-26 previously presented for examination remain in the application. No claims have been amended, canceled or added.

Claims 1-26 stand rejected under 35 U.S.C. § 102(a) as being considered to be anticipated by U.S. Patent No. 6,237,129 to Patterson et al. ("Patterson").

For a 35 U.S.C. §102 reference to anticipate a claim, the reference must teach every element of the claim. Section 2131 of the MPEP recites: "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California,* 814 F.2d 628, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

With respect to independent claim 1, Applicants teach and claim: "A method comprising: representing each vector associated with an integrated circuit datapath design as one of a row and a column in a graphical interface; and representing each bit slice associated with the integrated circuit datapath design in an orthogonal manner to the vectors in the graphical interface, the corresponding vector and bit slice representation in the graphical interface being different than an associated physical layout." The graphical interface enables a user to view and/or more easily manipulate the layout of an integrated circuit. See, for example, specification at paragraph [0013].

Patterson discloses a method for constraining circuit element positions in structured layouts. In particular, Patterson discloses a method whereby

placement information for elements of a logic module is specified in such a manner that specific coordinates need not be included. Instead, key words or phrases such as "COLUMN" or "ROW" indicate the manner in which the elements of the module are to be placed. Use of such parametric words or phrases are indicated as being intended to remove from the module developer the burden of determining exactly how large the module will be for each parameter combination, and in some cases, finding expressions by which the relative locations can be established. The method of Patterson is described as being applicable to any module or other element having an associated placement in a programmable device (e.g. a Field Programmable Gate Array or FPGA). (See e.g. Patterson, Abstract).

Patterson does not teach or disclose "a graphical interface" as required by claim 1. Instead, Patterson specifically and repeatedly refers to the use of phrases or expressions to specify the manner in which elements of a module are to be placed. (see e.g. Patterson Abstract, col. 4, lines 25-57 as examples). For at least this reason, Patterson cannot be considered to anticipate claim 1.

Each of the other pending independent claims 7, 18, and 23 recites limitations that are similar to the limitations of claim 1, although some differences may exist among the limitations of the other pending independent claims. These similar limitations nevertheless patentably distinguish claims 7, 18 and 23 over Patterson. Therefore, for at least these reasons, Applicants respectfully submit that Patterson does not anticipate all elements of independent claims 1, 7, 18, and 23.

Claims 2-6 depend from and further limit independent claim 1. Claims 8-17 depend from and further limit independent claim 7. Claims 19-22 depend from and further limit independent claim 18. Claims 24-26 depend from and further limit independent claim 23. Thus, for at least the same reasons advanced above with respect to independent claims 1, 7, 18, and 23, Applicants respectfully submit that Patterson does not anticipate all elements of dependent claims 2-6, 8-17, 19-22, and 24-26.

Based on the foregoing, applicants respectfully submit that the applicable rejections have been overcome and that claims 1-26 are in condition for allowance. If the Examiner disagrees or believes that further discussion will expedite prosecution of this case, the examiner is invited to telephone applicants' representative at the number indicated below.

If there are any charges, please charge Deposit Account No. 02-2666.

Respectfully submitted,

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